PCF8562

Universal LCD driver for low multiplex rates

Rev. 02 — 22 January 2007 Product data sheet

1. General description

The PCF8562 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 32 segments. The PCF8562 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional I^2C-bus. Communication overheads are minimized by a display RAM with auto-incremental addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

2. Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, $\frac{1}{2}$ and $\frac{1}{3}$
- Internal LCD bias generation with voltage-follower buffers
- 32 segment drives: up to sixteen 8-segment numeric characters; up to eight 15-segment alphanumeric characters; or any graphics of up to 128 elements
- 32 $\times$ 4-bit RAM for display data storage
- Auto-incremental display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- Independent supplies possible for LCD and logic voltages
- Wide power supply range: from 1.8 V to 5.5 V
- Wide logic LCD supply range: from 2.5 V for low-threshold LCDs and up to 6.5 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low-power consumption
- 400 kHz I^2C-bus interface
- Transistor-Transistor Logic (TTL)/CMOS compatible
- Compatible with 4-bit, 8-bit or 16-bit microprocessors or microcontrollers
- No external components
- Compatible with chip-on-glass technology
- Manufactured using silicon gate CMOS process

3. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCF8562TT	PCF8562TT	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

4. Block diagram

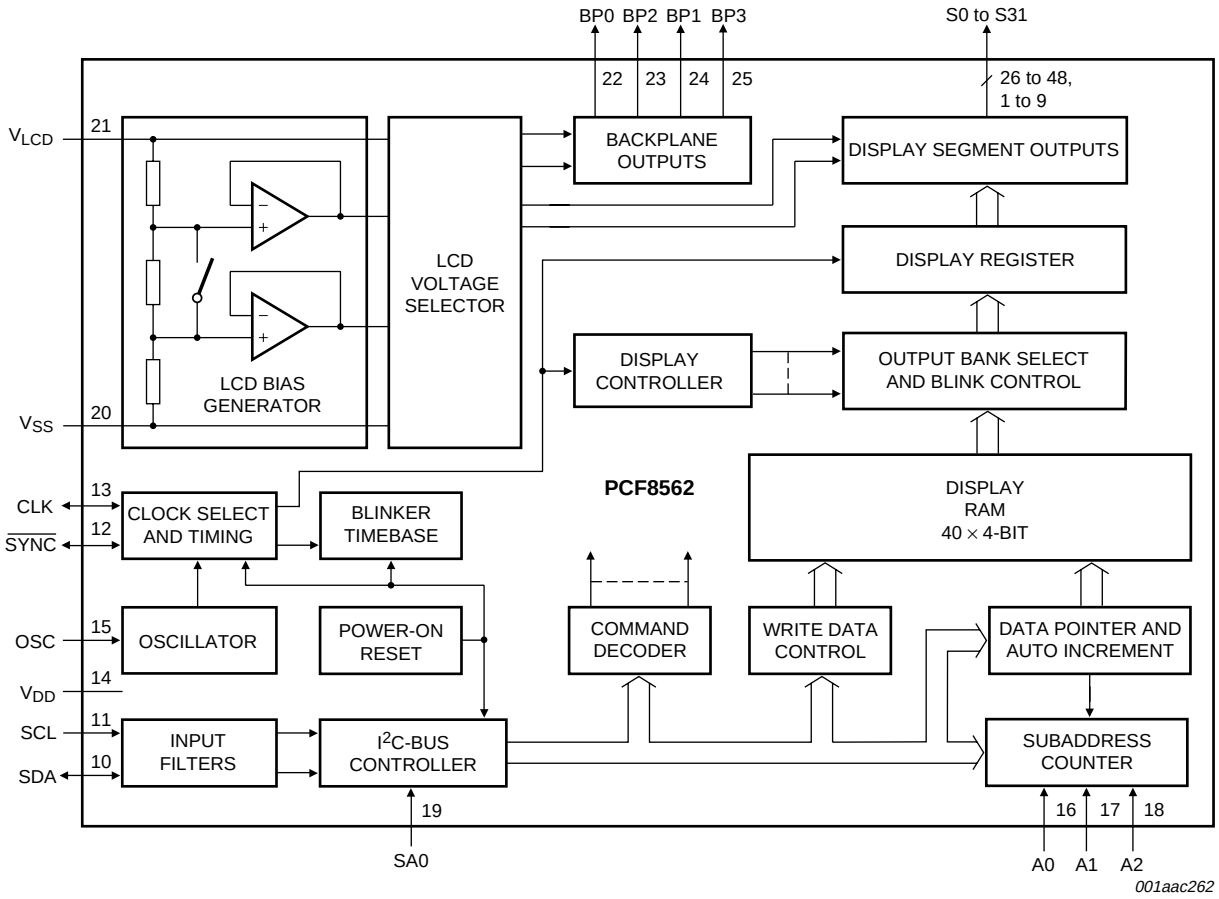


Fig 1. Block diagram

5. Pinning information

5.1 Pinning

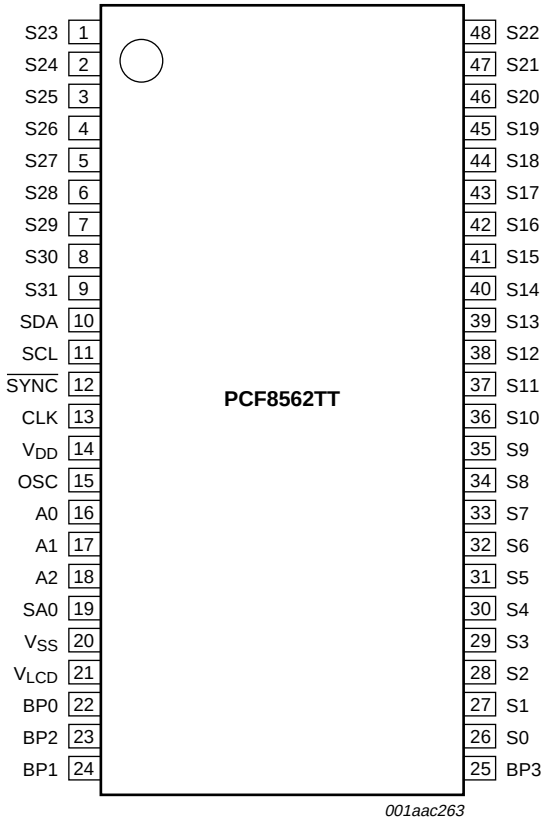


Fig 2. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
S23	1	LCD segment output
S24	2	LCD segment output
S25	3	LCD segment output
S26	4	LCD segment output
S27	5	LCD segment output
S28	6	LCD segment output
S29	7	LCD segment output
S30	8	LCD segment output
S31	9	LCD segment output
SDA	10	I^2C-bus serial data input and output
SCL	11	I^2C-bus serial clock input

Table 2. Pin description *…continued*

Symbol	Pin	Description
$\overline{SYNC}$	12	cascade synchronization input and output
CLK	13	external clock input and output
V_{DD}	14	supply voltage
OSC	15	internal oscillator enable input
A0	16	subaddress input
A1	17	subaddress input
A2	18	subaddress input
SA0	19	I^2C-bus slave address input: bit 0
V_{SS}	20	logic ground
V_{LCD}	21	LCD supply voltage
BP0	22	LCD backplane output
BP2	23	LCD backplane output
BP1	24	LCD backplane output
BP3	25	LCD backplane output
S0	26	LCD segment output
S1	27	LCD segment output
S2	28	LCD segment output
S3	29	LCD segment output
S4	30	LCD segment output
S5	31	LCD segment output
S6	32	LCD segment output
S7	33	LCD segment output
S8	34	LCD segment output
S9	35	LCD segment output
S10	36	LCD segment output
S11	37	LCD segment output
S12	38	LCD segment output
S13	39	LCD segment output
S14	40	LCD segment output
S15	41	LCD segment output
S16	42	LCD segment output
S17	43	LCD segment output
S18	44	LCD segment output
S19	45	LCD segment output
S20	46	LCD segment output
S21	47	LCD segment output
S22	48	LCD segment output

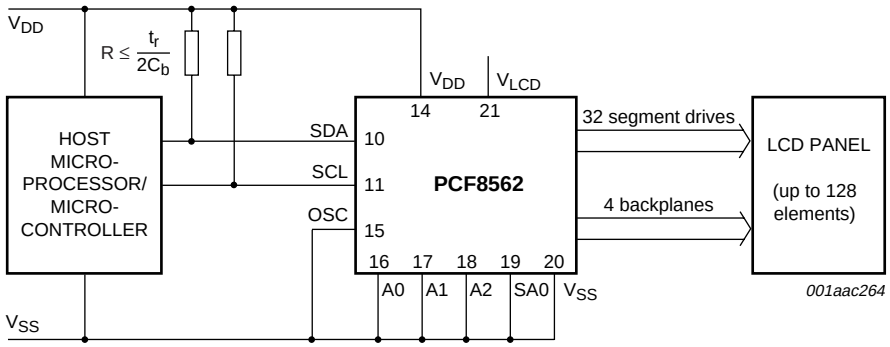
6. Functional description

The PCF8562 is a versatile peripheral device designed to interface between any microprocessor/microcontroller and a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 32 segments.

The display configurations possible with the PCF8562 depend on the number of active backplane outputs required. A selection of display configurations is shown in Table 3; all of these configurations can be implemented in the typical system shown in Figure 3.

Table 3. Selection of display configurations

Number of		7-segments numeric		14-segments alphanumeric		Dot matrix
Backplanes	Segments	Digits	Indicator symbols	Characters	Indicator symbols	
4	128	16	16	8	16	128 dots (4×32)
3	96	12	12	6	12	96 dots (3×32)
2	64	8	8	4	8	64 dots (2×32)
1	32	4	4	2	4	32 dots (1×32)



The resistance of the power supply lines must be kept to a minimum.

Fig 3. Typical system configuration

The host microprocessor/microcontroller maintains the 2-line I^2C-bus communication channel with the PCF8562. The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and the LCD panel chosen for the application.

6.1 Power-on reset

At power-on the PCF8562 resets to the following starting conditions:

- All backplane outputs are set to V_{LCD}
- All segment outputs are set to V_{LCD}
- Drive mode '1 : 4 multiplex with $\frac{1}{3}$ bias' is selected
- Blinking is switched off
- Input and output bank selectors are reset (as defined in Table 6)
- The I^2C-bus interface is initialized
- The data pointer and the subaddress counter are cleared
- Display is disabled

Data transfers on the I^2C-bus should be avoided for 1 ms following power-on to allow completion of the reset action.

6.2 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider comprising three resistors connected in series between V_{LCD} and V_{SS}. The middle resistor can be bypassed to provide a $\frac{1}{2}$ bias voltage level for the 1 : 2 multiplex configuration. The LCD voltage can be temperature compensated externally via the supply to pin V_{LCD}.

6.3 LCD voltage selector

The LCD voltage selector co-ordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting Discrimination ratios (D), are given in Table 4.

Table 4. Discrimination ratios

LCD drive mode	Number of		LCD bias configuration	$\frac{V_{off(rms)}}{V_{LCD}}$	$\frac{V_{on(rms)}}{V_{LCD}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
	Backplanes	Levels				
static	1	2	static	0	1	∞
1 : 2 multiplex	2	3	$\frac{1}{2}$	0.354	0.791	2.236
1 : 2 multiplex	2	4	$\frac{1}{3}$	0.333	0.745	2.236
1 : 3 multiplex	3	4	$\frac{1}{3}$	0.333	0.638	1.915
1 : 4 multiplex	4	4	$\frac{1}{3}$	0.333	0.577	1.732

A practical value for V_{LCD} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode a suitable choice is $V_{LCD} > 3V_{th}$.

Multiplex drive modes of 1 : 3 and 1 : 4 with $\frac{1}{2}$ bias are possible but the discrimination and hence the contrast ratios are smaller.

6.3.1 LCD bias formulae

Bias is calculated by the formula $\frac{1}{1+a}$

where for ½ bias, a = 1; for ⅓ bias, a = 2.

The LCD on voltage (V_{on}) is calculated using the formula: $V_{op}\sqrt{\frac{\frac{1}{N}+\left[(N-1)\times\left(\frac{1}{1+a}\right)\right]^2}{N}}$.

The LCD off voltage (V_{off}) is calculated using the formula: $V_{op}\sqrt{\frac{a^2-(2a+N)}{N\times(1+a)^2}}$

where V_{op} is the resultant voltage at the LCD segment; N is the LCD drive mode: 1 = static, 2 = 1 : 2, 3 = 1 : 3, 4 = 1 : 4.

Discrimination is the ratio of V_{on} to V_{off}, and is determined by the formula:

$$\frac{V_{ON}}{V_{OFF}} = \sqrt{\frac{(a+1)^2+(N-1)}{(a-1)^2+(N-1)}} \quad (1)$$

Using Equation 1 the discrimination for an LCD drive mode of 1 : 3 with ½ bias is:

$\sqrt{3}$ = 1.732

and the discrimination for an LCD drive mode of 1 : 4 with ½ bias is $\frac{\sqrt{21}}{3}$ = 1.528.

The advantage of these LCD drive modes is a reduction of the LCD full-scale voltage V_{LCD} as follows:

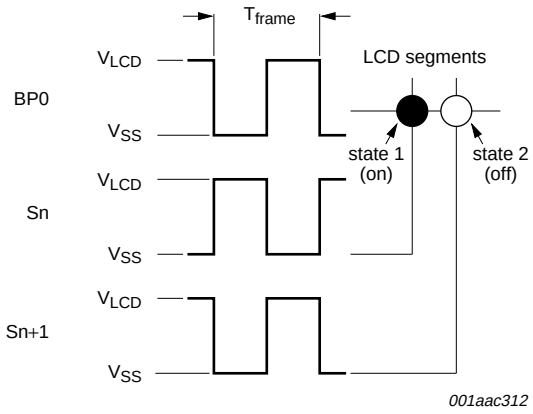
- 1 : 3 multiplex (½ bias): $V_{LCD} = \sqrt{6}\times V_{off(rms)}$ = 2.449 $V_{off(rms)}$
- 1 : 4 multiplex (½ bias): $V_{LCD} = \frac{(4\times\sqrt{3})}{3}$ = 2.309 $V_{off(rms)}$

These compare with V_{LCD} = 3 $V_{off(rms)}$ when ⅓ bias is used.

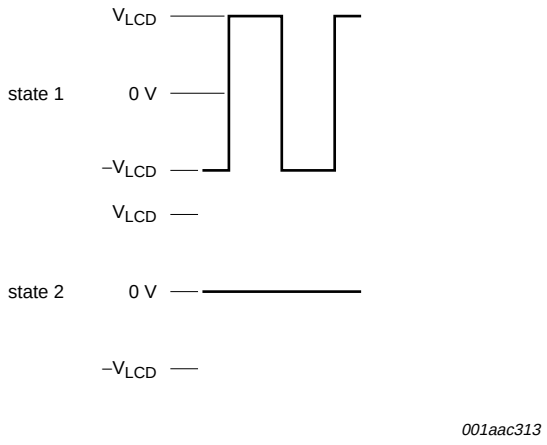
6.4 LCD drive mode waveforms

6.4.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. The backplane (BP0) and segment drive (Sn) waveforms for this mode are shown in Figure 4.



a. Waveforms at driver



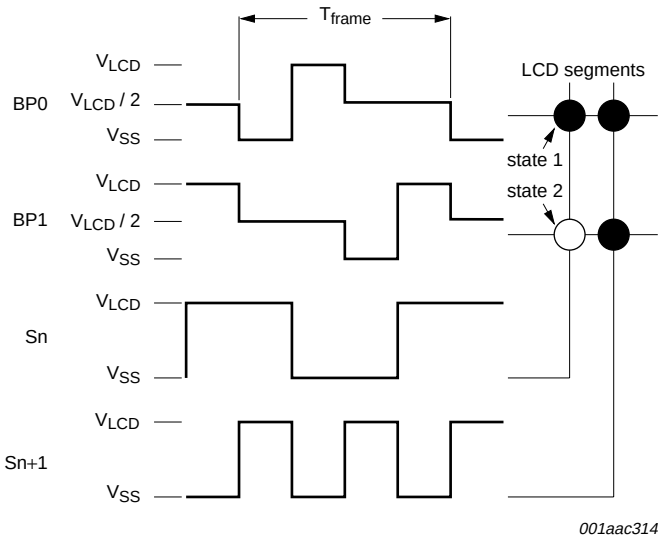
b. Resultant waveforms at LCD segment

$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$; $V_{on(rms)} = V_{LCD}$; $V_{state2}(t) = V_{Sn+1}(t) - V_{BP0}(t)$; $V_{off(rms)} = 0$ V

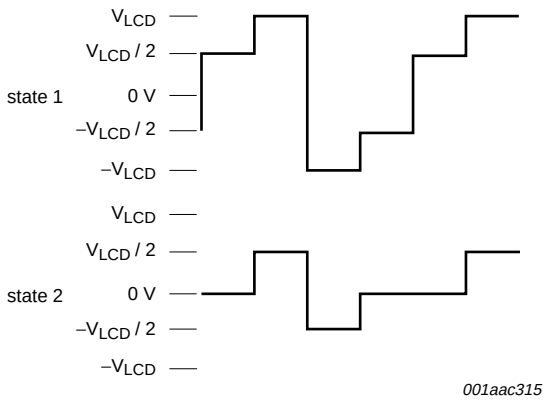
Fig 4. Static drive mode waveforms

6.4.2 1 : 2 multiplex drive mode

The 1 : 2 multiplex drive mode is used when two backplanes are provided in the LCD. This mode allows fractional LCD bias voltages of ½ bias or ⅓ bias as shown in Figure 5 and Figure 6.



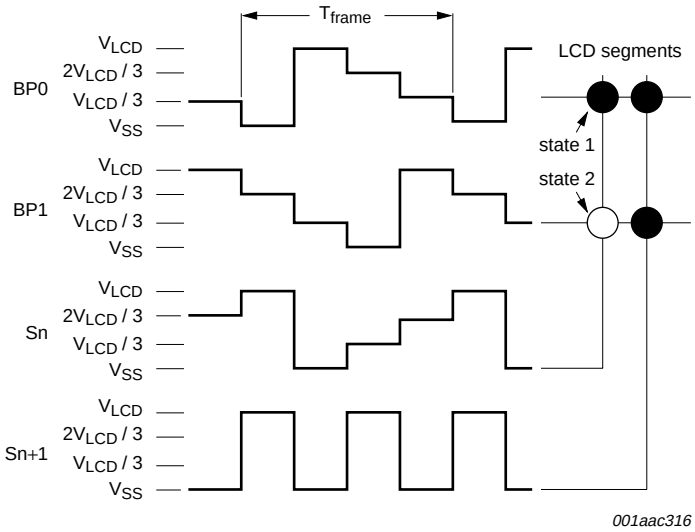
a. Waveforms at driver



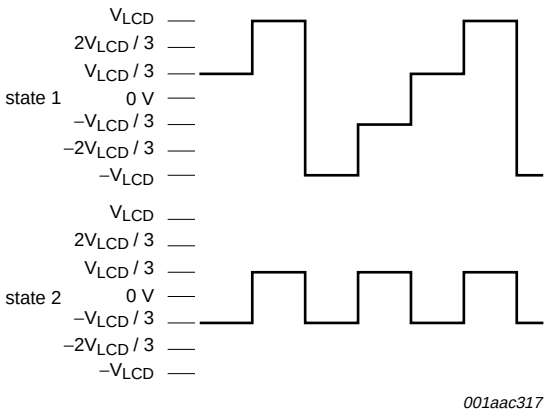
b. Resultant waveforms at LCD segment

$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$; $V_{on(rms)} = 0.791V_{LCD}$; $V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$; $V_{off(rms)} = 0.354V_{LCD}$

Fig 5. Waveforms for the 1 : 2 multiplex drive mode with ½ bias



a. Waveforms at driver



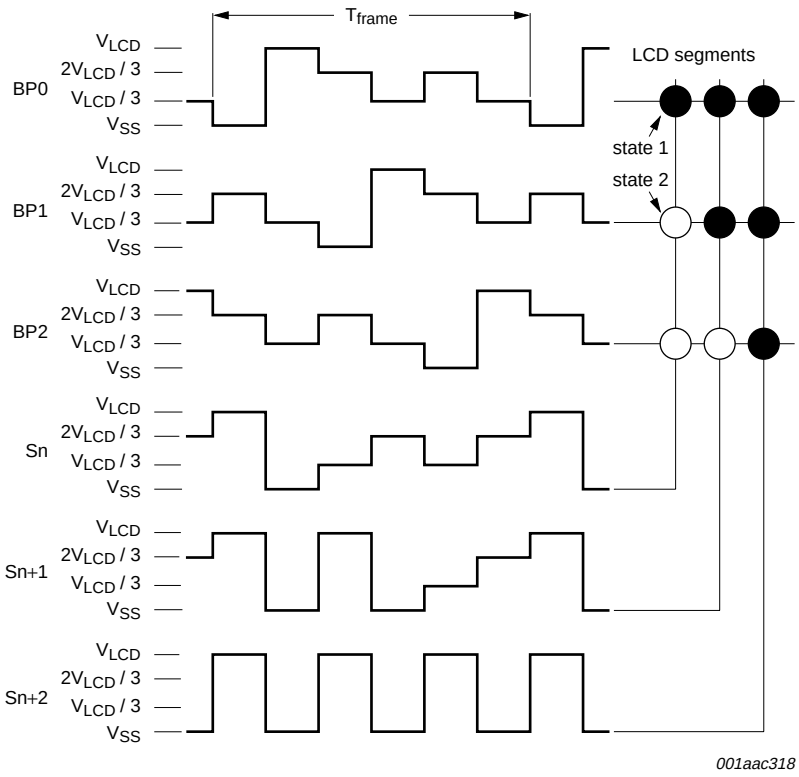
b. Resultant waveforms at LCD segment

$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$; $V_{on(rms)} = 0.745V_{LCD}$; $V_{state2}(t) = V_{Sn+1}(t) - V_{BP1}(t)$; $V_{off(rms)} = 0.333V_{LCD}$

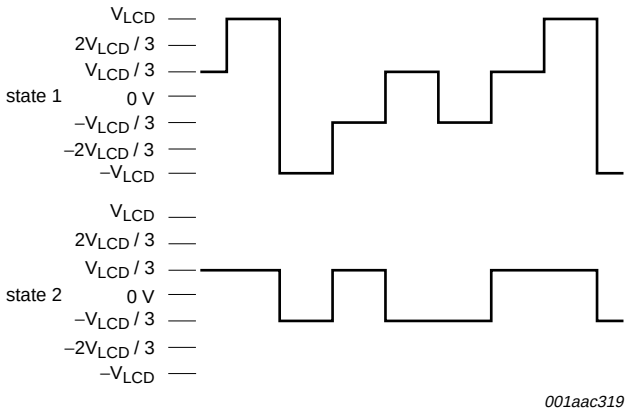
Fig 6. Waveforms for the 1 : 2 multiplex drive mode with $^1/_3$ bias

6.4.3 1 : 3 multiplex drive mode

When three backplanes are provided in the LCD, the 1 : 3 multiplex drive mode applies (see Figure 7).



a. Waveforms at driver



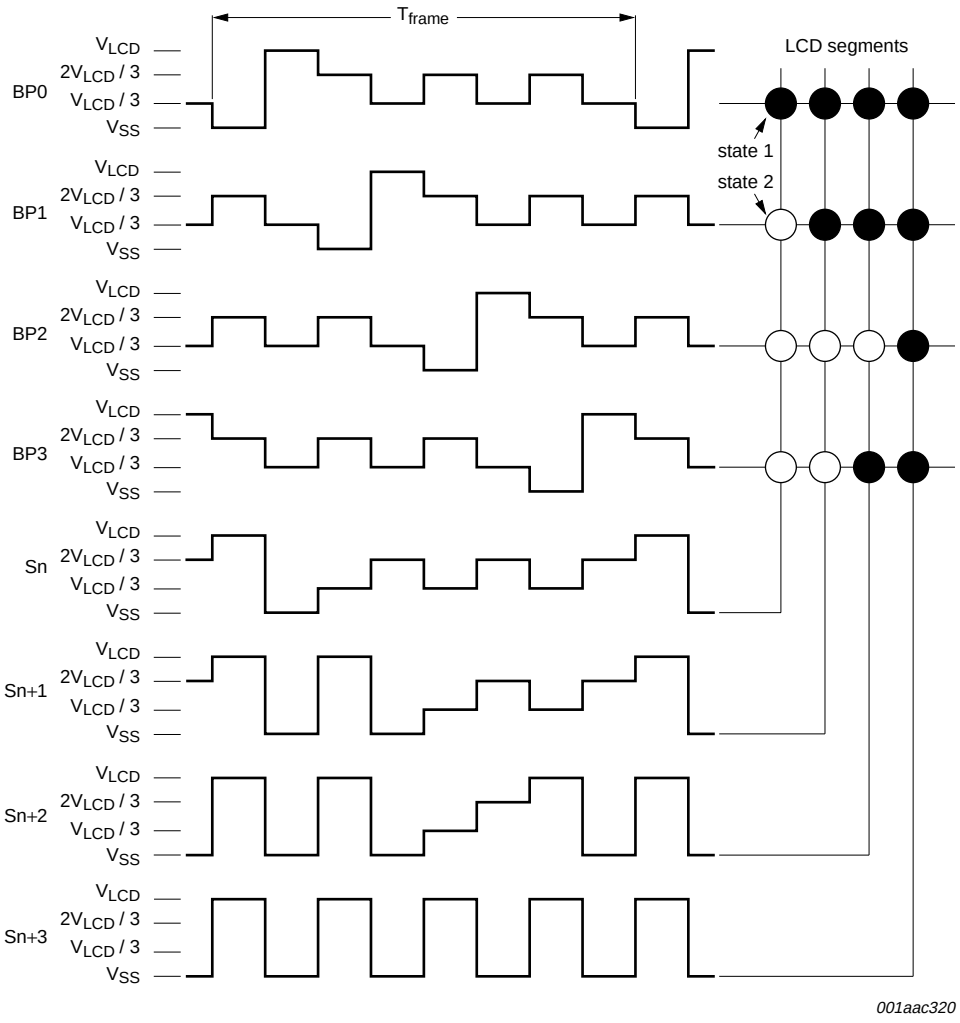
b. Resultant waveforms at LCD segment

$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$; $V_{on(rms)} = 0.638V_{LCD}$; $V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$; $V_{off(rms)} = 0.333V_{LCD}$

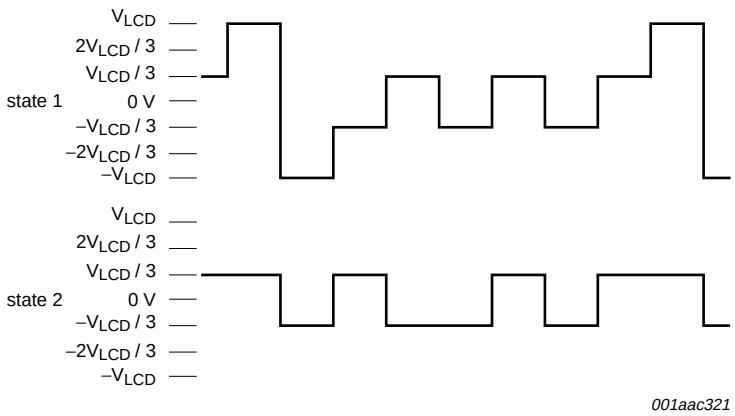
Fig 7. Waveforms for the 1 : 3 multiplex drive mode

6.4.4 1 : 4 multiplex drive mode

When four backplanes are provided in the LCD, the 1 : 4 multiplex drive mode applies (see Figure 8).



a. Waveforms at driver



b. Resultant waveforms at LCD segment

$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$; $V_{on(rms)} = 0.577V_{LCD}$; $V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$; $V_{off(rms)} = 0.333V_{LCD}$

Fig 8. Waveforms for the 1 : 4 multiplex drive mode

6.5 Oscillator

6.5.1 Internal clock

The internal logic of the PCF8562 and its LCD drive signals are timed either by its internal oscillator or by an external clock. The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. After power-up, pin SDA must be HIGH to guarantee that the clock starts.

6.5.2 External clock

Pin CLK is enabled as an external clock input by connecting pin OSC to V_{DD}.

The LCD frame signal frequency is determined by the clock frequency (f_{CLK}).

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

6.6 Timing

The PCF8562 timing controls the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. The timing also generates the LCD frame signal whose frequency is derived from the clock frequency. The frame signal frequency is a fixed division integer of the clock frequency (nominally 64 Hz) from either the internal or an external clock.

$$\text{Frame frequency} = \frac{f_{CLK}}{24}$$

6.7 Display register

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and each column of the display RAM.

6.8 Segment outputs

The LCD drive section includes 32 segment outputs S0 to S31 which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data residing in the display latch. When less than 32 segment outputs are required, the unused segment outputs should be left open-circuit.

6.9 Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required, the unused outputs can be left open-circuit. In the 1 : 3 multiplex drive mode, BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode, BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

6.10 Display RAM

The display RAM is a static 32 × 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the on-state of the corresponding LCD segment; similarly, a logic 0 indicates the off-state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 32 segments operated with respect to backplane BP0 (see Figure 9). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

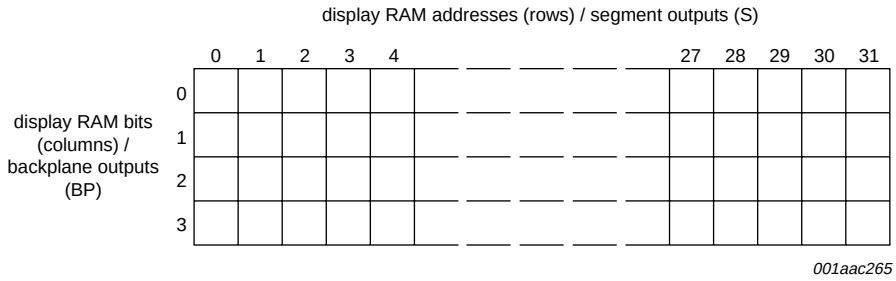


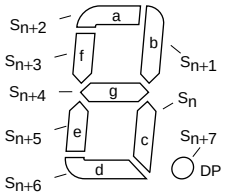
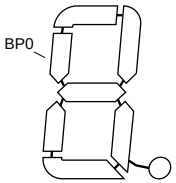
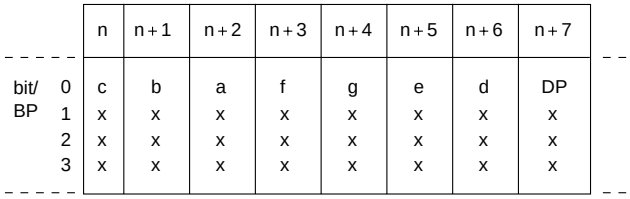
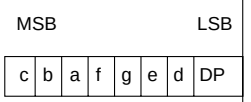
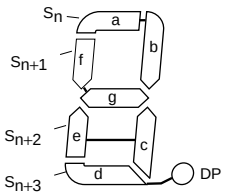
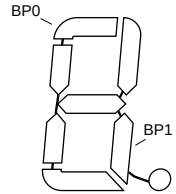
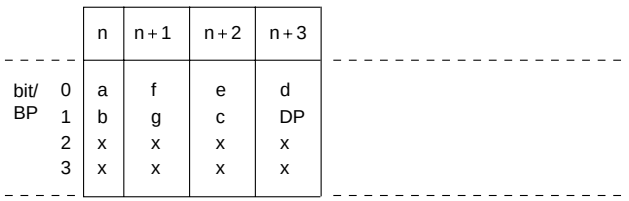
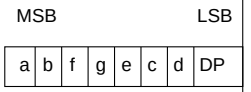
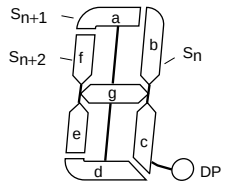
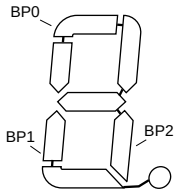
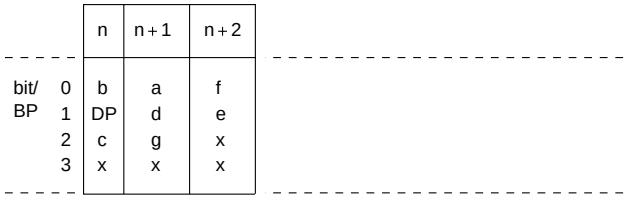
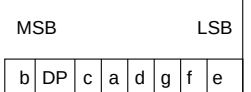
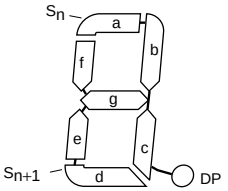
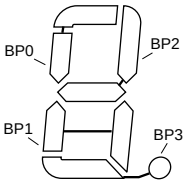
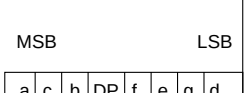
Fig 9. Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs also between bits in a RAM word and the backplane outputs

When display data is transmitted to the PCF8562, the display bytes received are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and does not wait for an acknowledge cycle as with the commands. Depending on the current multiplex drive mode, data is stored singularly, in pairs, triplets or quadruplets. For example, in the 1 : 2 mode, the RAM data is stored every second bit. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Figure 9; the RAM filling organization depicted applies equally to other LCD types.

With reference to Figure 9, in the static drive mode, the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 mode, the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 mode, these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted.

In the 1 : 4 mode, the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

6.11 Data pointer

drive mode	LCD segments	LCD backplanes	display RAM filling order	transmitted display byte
static				
1 : 2 multiplex				
1 : 3 multiplex				
1 : 4 multiplex				

mgl751

x = data bit unchanged.

Fig 10. Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C-bus

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the Load Data Pointer command. Following this, an arriving data byte is stored at the display RAM address indicated by the data pointer in accordance with the filling order shown in Figure 10. After each byte is stored, the contents of the data pointer are automatically incremented by a value dependent on the selected LCD drive mode: eight (static drive mode), four (1 : 2 mode), three (1 : 3 mode) or two (1 : 4 mode). If an I^2C-bus data access is terminated early then the state of the data pointer will be unknown. The data pointer should be re-written prior to further RAM access.

6.12 Device select

Storage is allowed to take place when the internal select register agrees with the hardware subaddress applied to A0, A1 and A2.

The hardware subaddress should not be changed whilst the device is being accessed on the I^2C-bus interface.

6.13 Output bank selector

The output bank selector selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the selected LCD drive mode and on the instant in the multiplex sequence. In 1 : 4 mode, all RAM addresses of bit 0 are selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 mode, bits 0, 1 and 2 are selected sequentially. In 1 : 2 mode, bits 0 and 1 are selected and, in static mode, bit 0 is selected. Signal $\overline{\text{SYNC}}$ will reset these sequences to the following starting points; bit 3 for 1 : 4 mode, bit 2 for 1 : 3 mode, bit 1 for 1 : 2 mode and bit 0 for static mode.

The PCF8562 includes a RAM bank switching feature in the static and 1 : 2 drive modes. In the static drive mode, the Bank Select command may request the contents of bit 2 to be selected for display instead of the contents of bit 0. In 1 : 2 mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This allows display information to be prepared in an alternative bank and then selected for display when it is assembled.

6.14 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. The Bank Select command can be used to load display data in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 mode. The input bank selector functions are independent of the output bank selector.

6.15 Blinker

The PCF8562 has a very versatile display blinking capability. The whole display can blink at a frequency selected by the Blink command. Each blink frequency is a multiple integer value of the clock frequency; the ratio between the clock frequency and blink frequency depends on the blink mode selected, as shown in Table 5.

Table 5. Blinking frequencies

Blink mode	Normal operating mode ratio	Nominal blink frequency
Off	-	blinking off
2 Hz[1]	$\frac{f_{CLK}}{768}$	2 Hz[1]
1 Hz[1]	$\frac{f_{CLK}}{1536}$	1 Hz[1]
0.5 Hz[1]	$\frac{f_{CLK}}{3072}$	0.5 Hz[1]

[1] Blink modes 0.5 Hz, 1 Hz and 2 Hz, and nominal blink frequencies 0.5 Hz, 1 Hz and 2 Hz correspond to an oscillator frequency (f_{CLK}) of 1536 Hz at pin CLK. The oscillator frequency range is given in Section 11.

An additional feature allows an arbitrary selection of LCD segments to be blinked in the static and 1 : 2 drive modes. This is implemented without any communication overheads by the output bank selector which alternates the displayed data between the data in the display RAM bank and the data in an alternative RAM bank at the blink frequency. This mode can also be implemented by the Blink command.

In the 1 : 3 and 1 : 4 drive modes, where no alternative RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

The entire display can be blinked at a frequency other than the nominal blink frequency by sequentially resetting and setting the display enable bit E at the required rate using the Mode Set command.

7. Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data Line (SDA) and a Serial Clock Line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

In chip-on-glass applications where the track resistance from the SDA pad to the system SDA line can be significant, a potential divider is generated by the bus pull-up resistor and the Indium Tin Oxide (ITO) track resistance. It is therefore necessary to minimize the track resistance from the SDA pad to the system SDA line to guarantee a valid LOW-level during the acknowledge cycle.

7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see Figure 11).

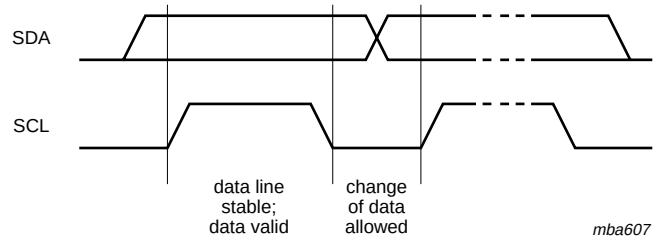


Fig 11. Bit transfer

7.2 Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P), (see Figure 12).

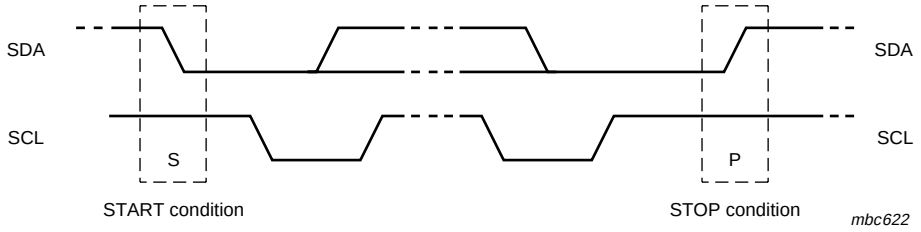


Fig 12. Definition of Start and Stop conditions

7.3 System configuration

A device generating a message is a ‘transmitter’, a device receiving a message is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’, (see Figure 13).

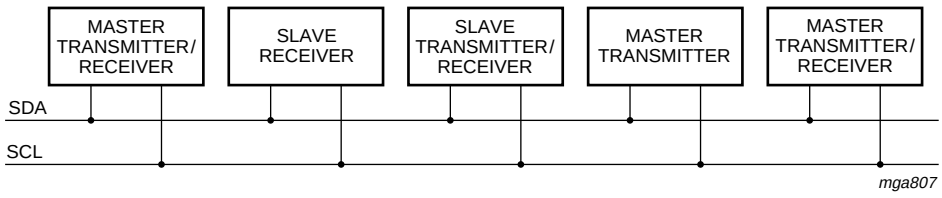


Fig 13. System configuration

7.4 Acknowledge

The number of data bytes that can be transferred from transmitter to receiver between the Start and Stop conditions is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH-level signal on the bus that is asserted by the transmitter during which time the master generates an extra acknowledge related clock pulse. An addressed slave receiver must generate an acknowledge after receiving each byte. Also a master receiver must generate an acknowledge after receiving each byte that has been clocked out of the slave transmitter. The acknowledging device must pull-down the SDA line during the acknowledge clock pulse so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a Stop condition (see Figure 14).

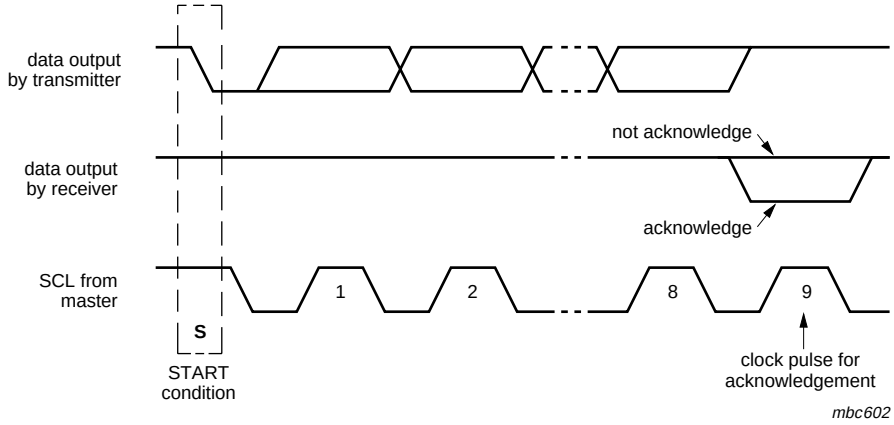


Fig 14. Acknowledgement on the I²C-bus

7.5 PCF8562 I²C-bus controller

The PCF8562 acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the PCF8562 are the acknowledge signals of the selected devices. Device selection depends on the I²C-bus slave address, on the transferred command data and on the hardware subaddress.

7.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.7 I²C-bus protocol

Two I²C-bus slave addresses (01110000 and 01110010) are reserved for the PCF8562. The least significant bit of the slave address that a PCF8562 will respond to is defined by the level tied to its SA0 input. The PCF8562 is a write-only device and will not respond to a read access.

The I²C-bus protocol is shown in Figure 15. The sequence is initiated with a Start condition (S) from the I²C-bus master which is followed by one of two possible PCF8562 slave addresses available. All PCF8562s whose SA0 inputs correspond to bit 0 of the slave address respond by asserting an acknowledge in parallel. This I²C-bus transfer is ignored by all PCF8562s whose SA0 inputs are set to the alternative level.

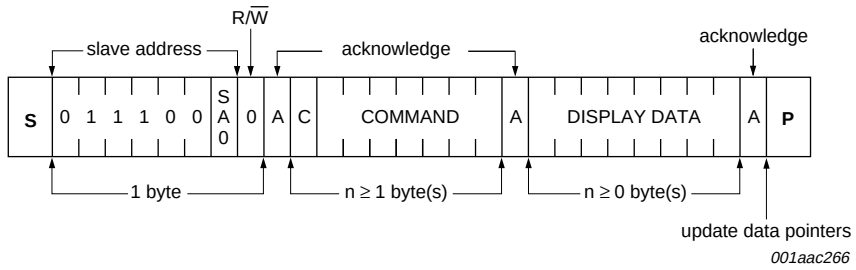
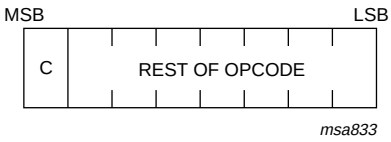


Fig 15. I²C-bus protocol

After an acknowledgement, one or more command bytes follow which define the status of the PCF8562.

The last command byte sent is identified by resetting its most significant bit, continuation bit C, (see Figure 16). The command bytes are also acknowledged by all addressed PCF8562s on the bus.



C = 0 = last command.

C = 1 = commands continue.

Fig 16. Format of command byte

After the last command byte, one or more display data bytes may follow. Display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated.

An acknowledgement after each byte is asserted only by PCF8562s that are addressed via address lines A0, A1 and A2. After the last display byte, the I²C-bus master asserts a Stop condition (P). Alternately a Start may be asserted to Restart an I²C-bus access.

7.8 Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. All available commands carry a continuation bit C in their most significant bit position as shown in Figure 16. When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If this bit is reset, it indicates that the command byte is the last in the transfer. Further bytes will be regarded as display data.

The five commands available to the PCF8562 are defined in Table 6.

Table 6. Definition of PCF8562 commands

Command	Operation code								Options	Description
Mode Set	C	1	0	[1]	E	B	M1	M0	Table 7	Defines LCD Drive mode.
									Table 8	Defines LCD bias configuration.
									Table 9	Defines display status; the possibility to disable the display allows implementation of blinking under external control.
Load Data Pointer	C	0	P5	P4	P3	P2	P1	P0	Table 10	6 bits of immediate data, bits P5 to P0 are transferred to the data pointer to define one of 32 display RAM addresses.
Device Select	C	1	1	0	0	A2	A1	A0	Table 11	3 bits of immediate data, bits A0 to A2 are transferred to the subaddress counter to define one of 8 hardware subaddresses.
Bank Select	C	1	1	1	1	0	I	O	Table 12	Defines the input bank selection (storage of arriving display data).
									Table 13	Defines the output bank selection (retrieval of LCD display data); the BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes.
Blink	C	1	1	1	0	A	BF1	BF0	Table 14	Defines the blink frequency
									Table 15	Selects the blink mode; normal operation with frequency set by BF1, BF0 or blinking by alternate display RAM banks; alternate RAM blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes.

[1] Not used.

Table 7. Mode set option 1

LCD drive mode		Bit	
Drive mode	Backplane	M1	M0
static	BP0	0	1
1 : 2	BP0, BP1	1	0
1 : 3	BP0, BP1, BP2	1	1
1 : 4	BP0, BP1, BP2, BP3	0	0

Table 8. Mode set option 2

LCD bias	Bit B
$\frac{1}{3}$ bias	0
$\frac{1}{2}$ bias	1

Table 9. Mode set option 3

Display status	Bit E
Disabled (blank)	0
Enabled	1

Table 10. Load data pointer option 1

Description	Bit					
Six bit binary value of 0 to 39	P5	P4	P3	P2	P1	P0

Table 11. Device select option 1

Description	Bit		
Three bit binary value of 0 to 7	A2	A1	A0

Table 12. Bank select option 1 (input)

Mode		Bit I
Static	1 : 2	
RAM bit 0	RAM bits 0 and 1	0
RAM bit 2	RAM bits 2 and 3	1

Table 13. Bank select option 2 (output)

Mode		Bit O
Static	1 : 2	
RAM bit 0	RAM bits 0 and 1	0
RAM bit 2	RAM bits 2 and 3	1

Table 14. Blink option 1

Blink frequency	Bit	
	BF1	BF0
off	0	0
2 Hz	0	1
1 Hz	1	0
0.5 Hz	1	1

Table 15. Mode set option 3

Blink mode	Bit A
Normal blinking	0
Alternate RAM bank blinking	1

7.9 Display controller

The display controller executes the commands identified by the command decoder. It contains the device's status registers and co-ordinates their effects. The display controller is also responsible for loading display data into the display RAM in the correct filling order.

7.10 Multiple chip operation

For large display configurations please refer to the PCF8576D device.

Please refer to PCF8576D if you need to drive more segments (> 128 elements).

The contact resistance between the $\overline{\text{SYNC}}$ input/output on each cascaded device must be controlled. If the resistance is too high, the device will not be able to synchronize properly; this is particularly applicable to chip-on-glass applications. The maximum $\overline{\text{SYNC}}$ contact resistance allowed for the number of devices in cascade is given in Table 16.

Table 16. $\overline{\text{SYNC}}$ contact resistance

Number of devices	Maximum contact resistance
2	6000 Ω
3 to 5	2200 Ω
6 to 10	1200 Ω
10 to 16	700 Ω

8. Device protection

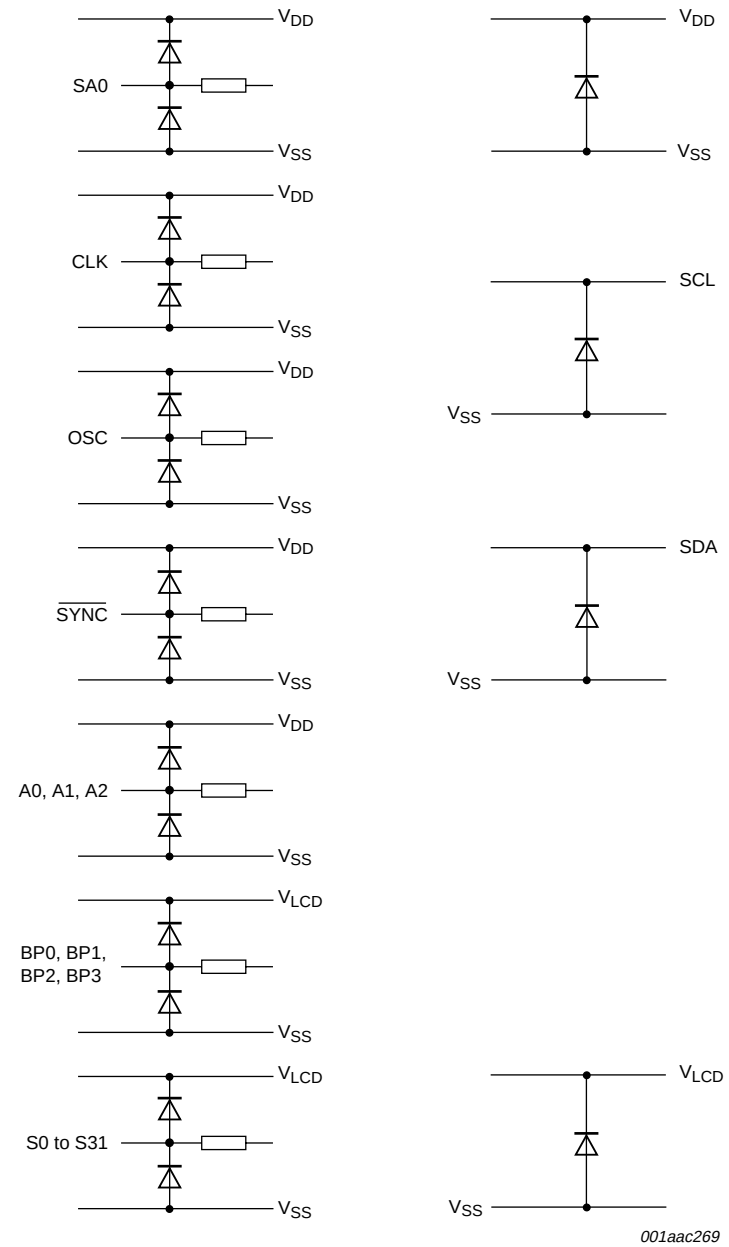


Fig 17. Device protection diagram

9. Limiting values

Table 17. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+6.5	V
V_{LCD}	LCD supply voltage		V_{SS} – 0.5	+7.5	V
V_i	input voltage	pins CLK, $\overline{SYNC}$, SA0, OSC, A2 to A0	V_{SS} – 0.5	V_{DD} + 0.5	V
		pins SCL and SDA	V_{SS} – 0.5	+6.5	V
V_O	output voltage	pins S31 to S0, BP3 to BP0	V_{SS} – 0.5	V_{DD} + 0.5	V
I_I	input current		–10	+10	mA
I_O	output current		–10	+10	mA
I_{DD}	supply current		–50	+50	mA
I_{SS}	ground current		–50	+50	mA
I_{LCD}	LCD supply current		–50	+50	mA
P_{tot}	total power dissipation		-	400	mW
P/out	power dissipation per output		-	100	mW
T_{stg}	storage temperature		–65	+150	°C

9.1 ESD values

- Electrostatic Discharge (ESD) protection exceeds 2000 V Human Body Model (HBM) per JESD22-A114, 200 V Machine Model (MM) per JESD22-A115 and 2000 V Charged Device Model (CDM) per JESD22-C101.
- Latch-up testing is done to JEDEC standard JESD78 which exceeds 100 mA.

10. Static characteristics

Table 18. Static characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 6.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage			1.8	-	5.5	V
V_{LCD}	LCD supply voltage		[1]	2.5	-	6.5	V
I_{DD}	supply current	f_{CLK} = 1536 Hz	[2]	-	8	20	µA
I_{LCD}	LCD supply current	f_{CLK} = 1536 Hz	[2]	-	24	60	µA
Logic							
V_{IL}	LOW-level input voltage	pins SCL, SDA		V_{SS}	-	$0.3V_{DD}$	V
		pins CLK, $\overline{SYNC}$, OSC, A2 to A0 and SA0		V_{SS}	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage	pins SCL, SDA	[3]	$0.7V_{DD}$	-	V_{DD}	V
		pins CLK, $\overline{SYNC}$, OSC, A2 to A0 and SA0		$0.7V_{DD}$	-	V_{DD}	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 5 V					
		pins CLK, $\overline{SYNC}$		1	-	-	mA
		pin SDA		3	-	-	mA
I_{OH}	HIGH-level output current	pin CLK; V_{OH} = 4.6 V; V_{DD} = 5 V		−1	-	-	mA
I_L	leakage current	pins CLK, SCL, SDA, A2 to A0 and SA0; $V_i = V_{DD}$ or V_{SS}		−1	-	+1	µA
		pin OSC; $V_i = V_{DD}$		−1	-	+1	µA
V_{POR}	power-on reset voltage level			1.0	1.3	1.6	V
C_i	input capacitance		[4]	-	-	7	pF
LCD outputs							
V_{TOL}	DC voltage tolerance	pins BP3 to BP0		−100	-	+100	mV
		pins S31 to S0		−100	-	+100	mV
R_O	output resistance	V_{LCD} = 5 V					
		pins BP3 to BP0	[5]	-	1.5	-	kΩ
		pins S31 to S0	[5]	-	6.0	-	kΩ

[1] V_{LCD} > 3 V for ⅓ bias.

[2] LCD outputs are open-circuit; inputs at V_{SS} or V_{DD}; external clock with 50 % duty factor; I^2C-bus inactive.

[3] When tested, I^2C-bus pins SCL and SDA have no diode to V_{DD} and may be driven according to the V_i limiting values given in Section 9; also see Figure 17.

[4] Periodically sampled, not 100 % tested.

[5] Outputs measured one at a time.

11. Dynamic characteristics

Table 19. Dynamic characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 6.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{CLK}	oscillator frequency		[1]	960	1890	2640	Hz
t_{CLKH}	input CLK HIGH time			60	-	-	µs
t_{CLKL}	input CLK LOW time			60	-	-	µs
$t_{PD(\overline{SYNC})}$	$\overline{SYNC}$ propagation delay			-	30	-	ns
$t_{\overline{SYNCL}}$	$\overline{SYNC}$ LOW time			1	-	-	µs
$t_{PD(LCD)}$	driver delays with test loads	V_{LCD} = 5 V	[2]	-	-	30	µs
Timing characteristics: I²C-bus[3]							
f_{SCL}	SCL clock frequency			-	-	400	kHz
t_{BUF}	bus free time between a STOP and START			1.3	-	-	µs
$t_{HD;STA}$	START condition hold time			0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	-	-	µs
t_{LOW}	SCL LOW time			1.3	-	-	µs
t_{HIGH}	SCL HIGH time			0.6	-	-	µs
t_r	SCL and SDA rise time	f_{SCL} = 400 kHz		-	-	0.3	µs
		f_{SCL} < 400 kHz		-	-	1.0	µs
t_f	SCL and SDA fall time			-	-	0.3	µs
C_b	capacitive load for each bus line			-	-	400	pF
$t_{SU;DAT}$	data set-up time			100	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	-	ns
$t_{SU;STO}$	set-up time for STOP condition			0.6	-	-	µs
t_{SP}	pulse width of spikes that must be suppressed by the input filter			-	-	50	ns

[1] Typical output duty factor: 50 % measured at the CLK output pin.

[2] Not tested in production.

[3] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

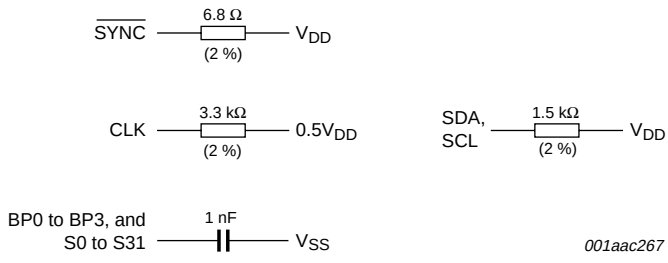


Fig 18. Test loads

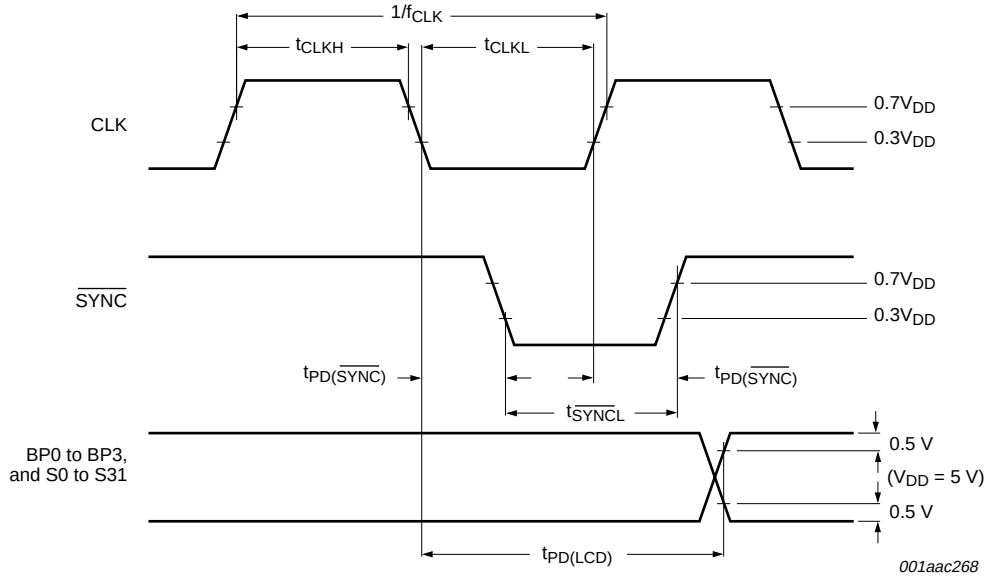


Fig 19. Driver timing waveforms

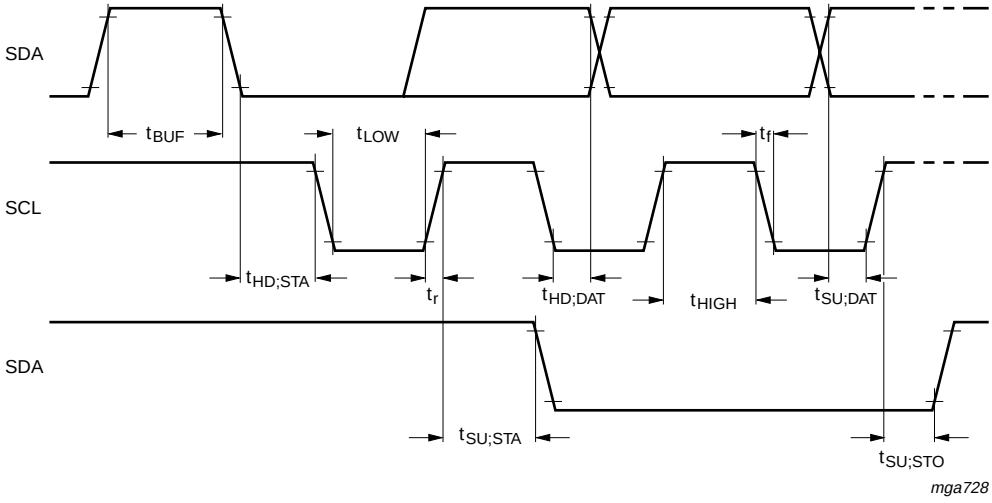
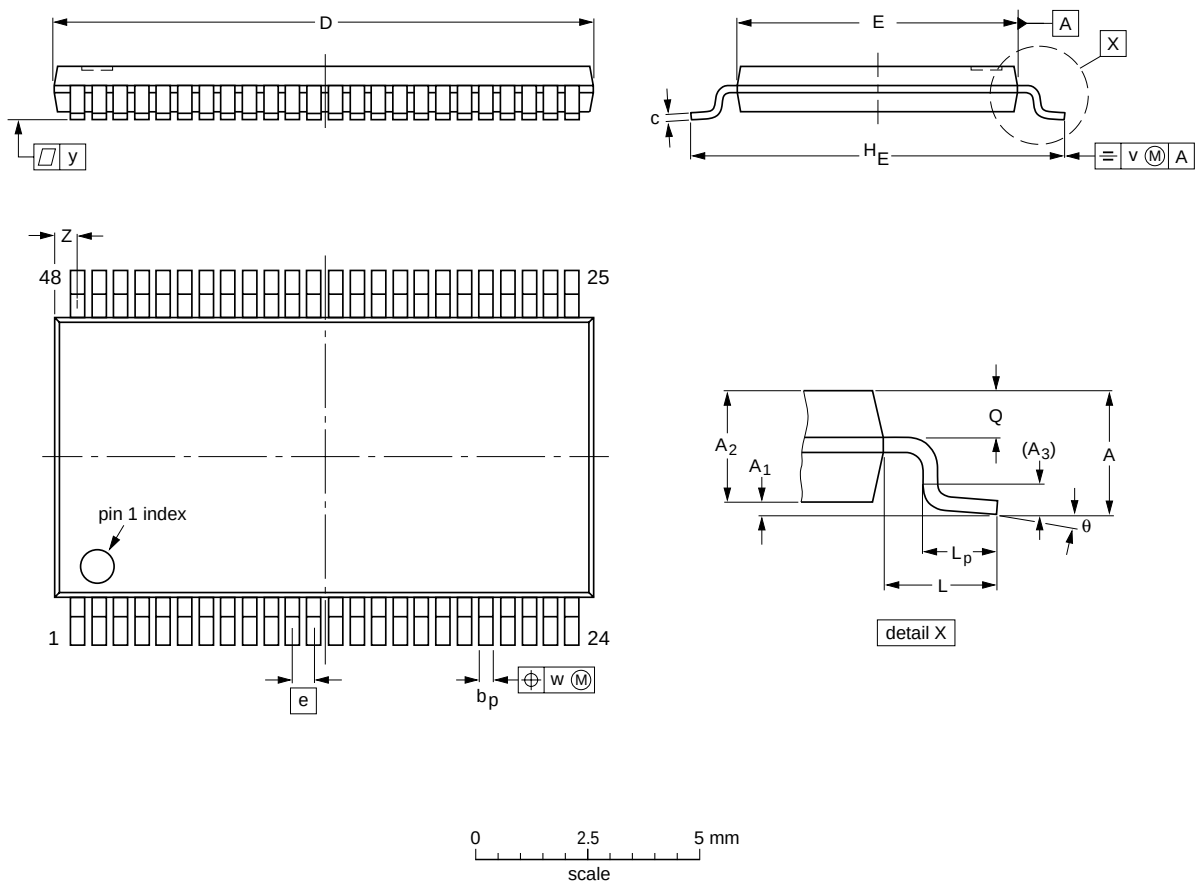


Fig 20. I²C-bus timing waveforms

12. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~99-12-27~~ 03-02-19

Fig 21. Package outline SOT362-1 (TSSOP48)

13. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling MOS devices; see *JESD625-A and/or IEC61340-5*.

14. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 22) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 20 and 21

Table 20. SnPb eutectic process (from J-STD-020C)

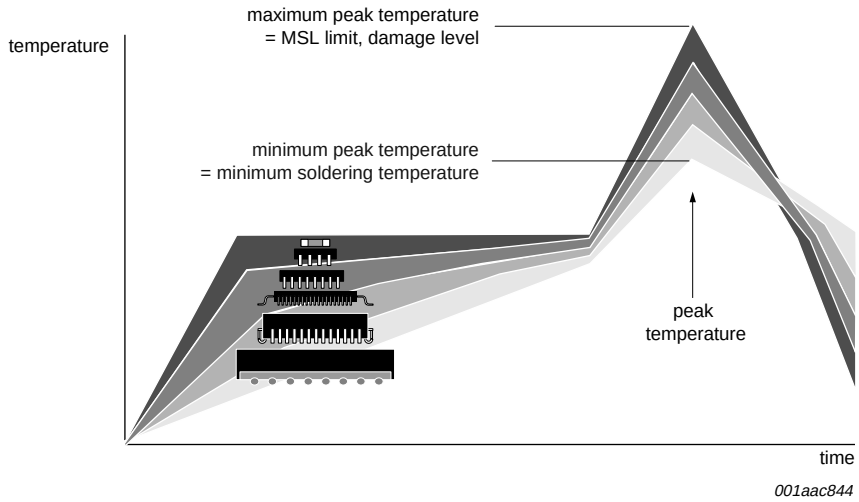
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 21. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 22.



MSL: Moisture Sensitivity Level

Fig 22. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

15. Revision history

Table 22. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF8562_2	20070122	Product data sheet	-	PCF8562_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 6.6: corrected typo: LCD frame frequency changed from 64 kHz to 64 Hz • Table 1: added column for 'topside mark'			
PCF8562_1	20050801	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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